REVISIONS			
LTR	DESCRIPTION	DATE (YY-MM-DD)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Thanh V. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY-MM-DD 02-11-07	**CHECKED BY** Thanh V. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, ADVANCED HIGH SPEED CMOS, HEX SCHMITT-TRIGGER INVERTER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/03605**
	REV	**PAGE** 1 **OF** 15

AMSC N/A

5962-V005-03

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance hex Schmitt-trigger inverter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03605	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	74AHC14-EP	Hex Schmitt-trigger inverter

1.2.2 Case outline(s). The case outlines shall be as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	MS-012	Plastic small-outline package
Y	14	MO-153	Plastic small-outline package

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to 7.0 V
Input voltage range (V_I) ..... -0.5 V to 7.0 V 2/
Output voltage range (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -20 mA
Output clamp current (I_{OK}) ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current (I_O) (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Package thermal impedance (θ_{JA}): 3/
X package ..... 86°C/W
Y package ..... 113°C/W

1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC}) ..... 2.0 V to 5.5 V
Input voltage range (V_I) ..... 0.0 V to 5.5 V
Output voltage range (V_O) ..... 0.0 V to V_{CC}
Maximum high level output current (I_{OH}):
V_{CC} = 2.0 V ..... -50 µA
V_{CC} = 3.3 V ± 0.3 V ..... -4.0 mA
V_{CC} = 5.0 V ± 0.5 V ..... -8.0 mA
Maximum low level output current (I_{OL}):
V_{CC} = 2.0 V ..... 50 µA
V_{CC} = 3.3 V ± 0.3 V ..... 4.0 mA
V_{CC} = 5.0 V ± 0.5 V ..... 8.0 mA
Operating free-air temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices
JEDEC STD 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at http://www.jedec.org)

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Truth table. The truth table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics.

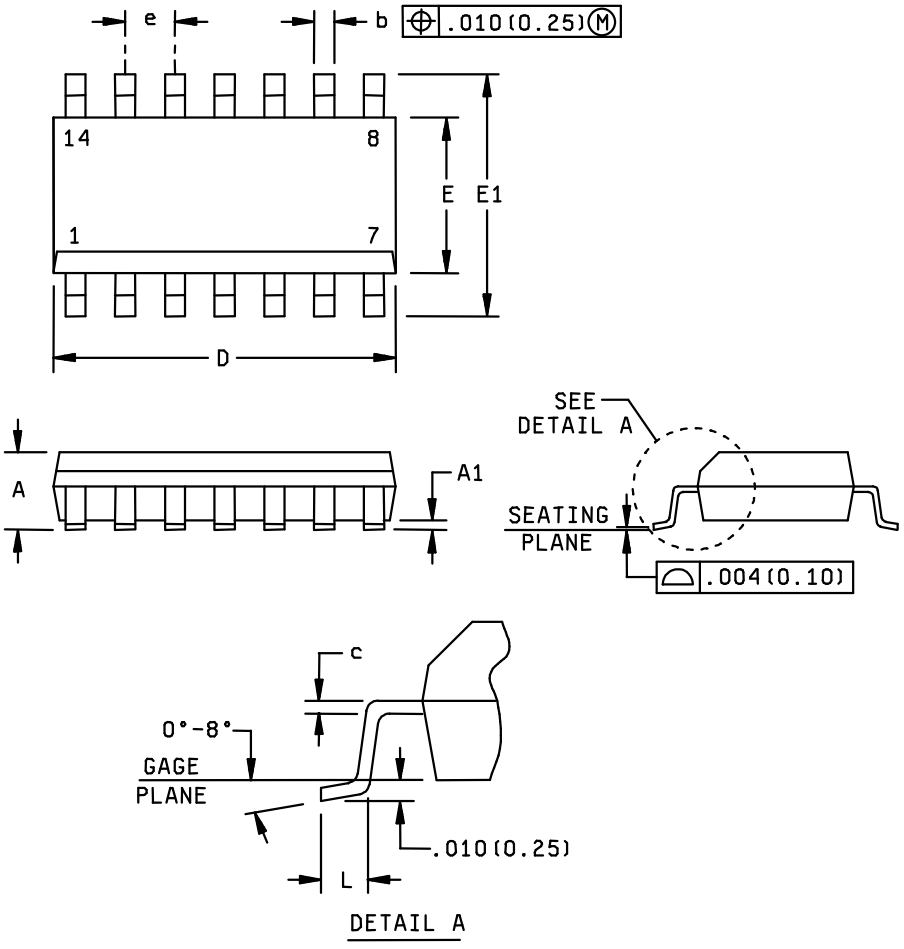
Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Positive-going input threshold voltage	V_{T+}		3.0 V	25°C, -55°C to 125°C	All	1.2	2.2	V
			4.5 V			1.75	3.15	
			5.5 V			2.15	3.85	
Negative-going input threshold voltage	V_{T-}		3.0 V	25°C, -55°C to 125°C	All	0.9	1.9	V
			4.5 V			1.35	2.75	
			5.5 V			1.65	3.35	
Hysteresis (V_{T+} - V_{T-})	ΔV_T		3.0 V	25°C, -55°C to 125°C	All	0.3	1.2	V
			4.5 V			0.4	1.4	
			5.5 V			0.5	1.6	
High level output voltage	V_{OH}	I_{OH} = -50 µA	2.0 V	25°C, -55°C to 125°C	All	1.9		V
			3.0 V			2.9		
			4.5 V			4.4		
		I_{OH} = -4 mA	3.0 V	25°C		2.58		
				-55°C to 125°C		2.48		
		I_{OH} = -8 mA	4.5 V	25°C		3.94		
				-55°C to 125°C		3.80		
Low level output voltage	V_{OL}	I_{OL} = 50 µA	2.0 V	25°C, -55°C to 125°C	All		0.1	V
			3.0 V				0.1	
			4.5 V				0.1	
		I_{OL} = 4 mA	3.0 V	25°C			0.36	
				-55°C to 125°C			0.5	
		I_{OL} = 8 mA	4.5 V	25°C			0.36	
				-55°C to 125°C			0.5	
Input current	I_I	V_I = 5.5 V or GND	0.0 V to 5.5 V	25°C	All		±0.1	µA
				-55°C to 125°C			±1.0	
Quiescent supply current	I_{CC}	V_I = V_{CC} or GND I_O = 0 A	5.5 V	25°C	All		2.0	µA
				-55°C to 125°C			20.0	

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	V_{CC}	Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$ 1/	C_L = 50 pF	5.0 V	25°C	All	0.8 typical		V
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$ 1/		5.0 V	25°C	All	-0.4 typical		V
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$ 1/		5.0 V	25°C	All	4.6 typical		V
High level dynamic input voltage	$V_{IH(D)}$ 1/		5.0 V	25°C	All	3.5		V
Low level dynamic input voltage	$V_{IL(D)}$ 1/		5.0 V	25°C	All		1.5	V
Input capacitance	C_I	V_I = V_{CC} or GND	5.0 V	25°C	All		10	pF
Power dissipation capacitance	C_{PD}	No load f = 1 MHz	5.0 V	25°C	All	9.0 typical		pF
Propagation delay time, A to Y	t_{PLH}, t_{PHL}	C_L = 15 pF See figure 5	3.0 V and 3.6 V	25°C	All		12.8	ns
				-55°C to 125°C		1.0	15.0	
			4.5 V and 5.5 V	25°C			8.6	
				-55°C to 125°C		1.0	10.0	
		C_L = 50 pF See figure 5	3.0 V and 3.6 V	25°C	All		16.3	
				-55°C to 125°C		1.0	18.5	
			4.5 V and 5.5 V	25°C			10.6	
				-55°C to 125°C		1.0	12.0	

1/ Characteristics are for surface-mount packages only.

Case X



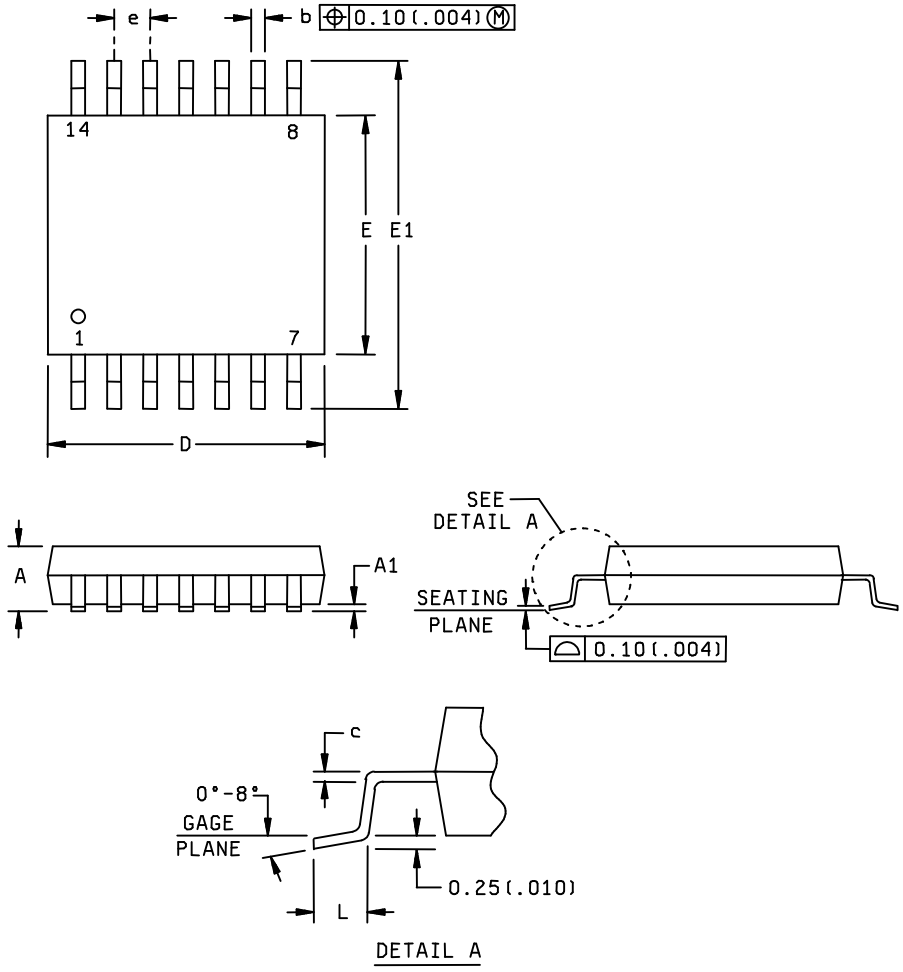
NOTES:
1. All linear dimensions are in inches (millimeters).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed .006 inches.
4. Fall within JEDEC MS-012.

FIGURE 1. Case outlines.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		.069		1.75
A1	.004	.010	0.10	0.25
b	.014	.020	0.35	0.51
c		.008 NOM		0.20 NOM
D	.337	.344	8.55	8.75
E	.150	.157	3.81	4.00
E1	.228	.244	5.80	6.20
e		.050 BSC		1.27 BSC
L	.016	.044	0.40	1.12

FIGURE 1. Case outlines - Continued.

Case Y



NOTES:
1. All linear dimensions are in millimeters (inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

Case Y - Continued

Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A		1.20		.047
A1	0.05	0.15	.002	.006
b	0.19	0.30	.007	.012
c		0.15 NOM		.006 NOM
D	4.90	5.10	.193	.201
E	4.30	4.50	.169	.177
E1	6.20	6.60	.244	.260
e		0.65 BSC		.026 BSC
L	0.50	0.75	.020	.030

FIGURE 1. Case outlines - Continued.

Inputs	Output
A	Y
H	L
L	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

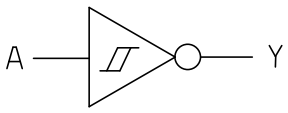


FIGURE 3. Logic diagram.

Device type 01	
Case outlines	X and Y
Terminal number	Terminal symbol
1	1A
2	1Y
3	2A
4	2Y
5	3A
6	3Y
7	GND
8	4Y
9	4A
10	5Y
11	5A
12	6Y
13	6A
14	V_{CC}

FIGURE 4. Terminal connections.

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
OPEN DRAIN	V_{CC}

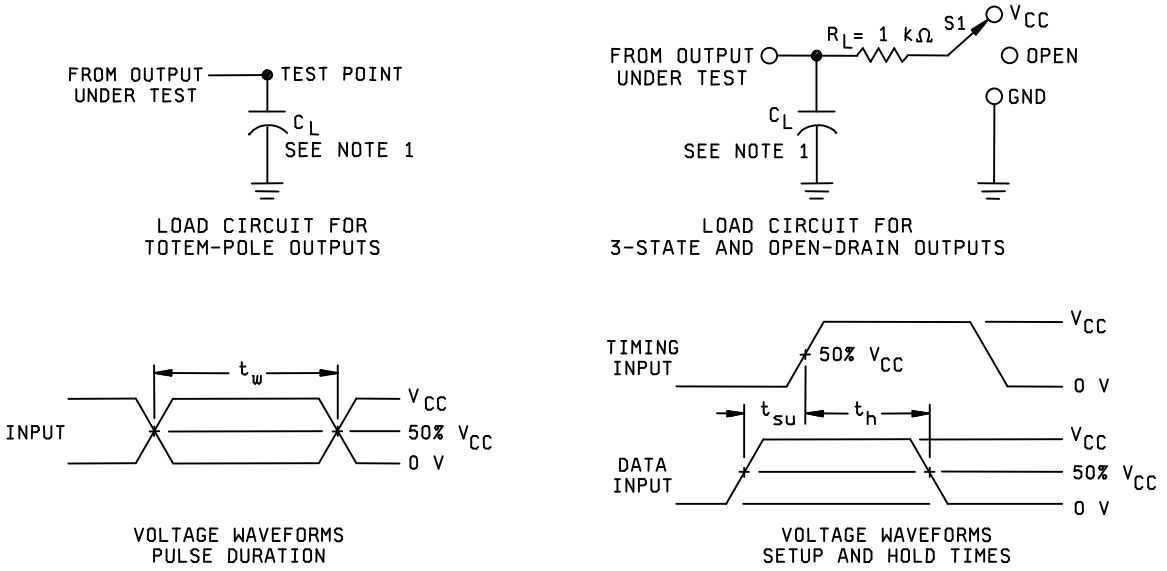
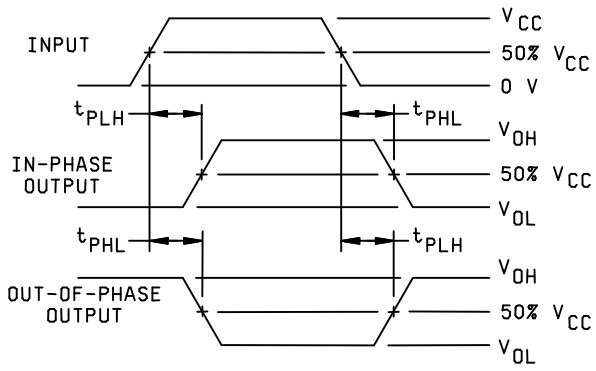
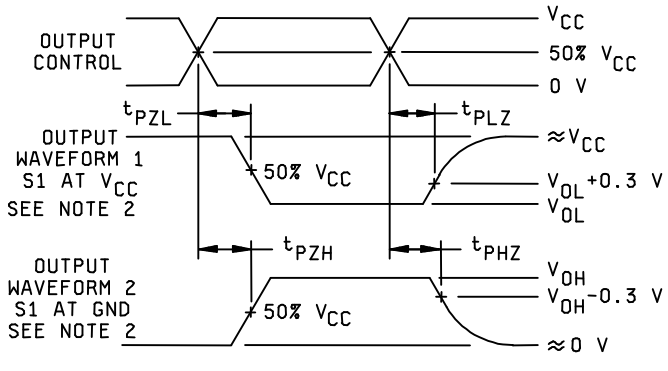


FIGURE 5. Test circuit and timing waveforms.



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
4. The outputs are measured one at a time with one input transition per measurement.

FIGURE 5. Test circuit and timing waveforms - Continued.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6.0 NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03605-01XE	01295	SN74AHC14MDREP	AHC14MEP
V62/03605-01YE	01295	SN74AHC14MPWREP	HA14MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493